

<b>Module Title:</b>	<b>CAD 1 – FPGA Design</b>
<b>Academic year:</b>	2009 – 2010
<b>Credit Value:</b>	4 – Elective
<b>Pre- requisites:</b>	None
<b>Assessment:</b>	85% Practical 15% Continuous Assessment (CA)
<b>Aims</b>	This subject introduces the student to FPGA design.
<b>Module Content</b>	<ul style="list-style-type: none"> <li>• Introduction</li> <li>• FPGA</li> <li>• VHDL</li> </ul>
<b>Intended Learning Outcomes:</b>	<p><b>On successful completion of the module the student will be expected to be able to:</b></p> <ol style="list-style-type: none"> <li>1. Develop and document a design using a structured design methodology.</li> <li>2. Describe FPGA and CPLD architecture and advantages.</li> <li>3. Create and simulate schematic based designs.</li> <li>4. Implement and test designs on FPGA/CPLD hardware.</li> <li>5. Use VHDL to model designs.</li> <li>6. Describe current developments in IC design, such as synthesis.</li> <li>7. Write reports.</li> </ol>